

Fig. 1

	<u>Inst</u>	<u>Hit/Miss</u>	<u>Data</u>	
18	LDR [R _n]	Hit	Data [R _n]	
	MOV	N/A	—	
	CMP	N/A	—	
	⋮	⋮	⋮	
20	LDR [R _n]	Miss	—	variable delay
	MOV	N/A	—	
	CMP	N/A	Data [R _n]	
	⋮			
22	LDR [R1]	Miss	—	
24	LDR [R2]	Miss	—	
	MOV	N/A	—	
	CMP	N/A		
	ADD	N/A		
28			Data [R2]	missed data is returned out of order
26			Data [R1]	

Fig. 2

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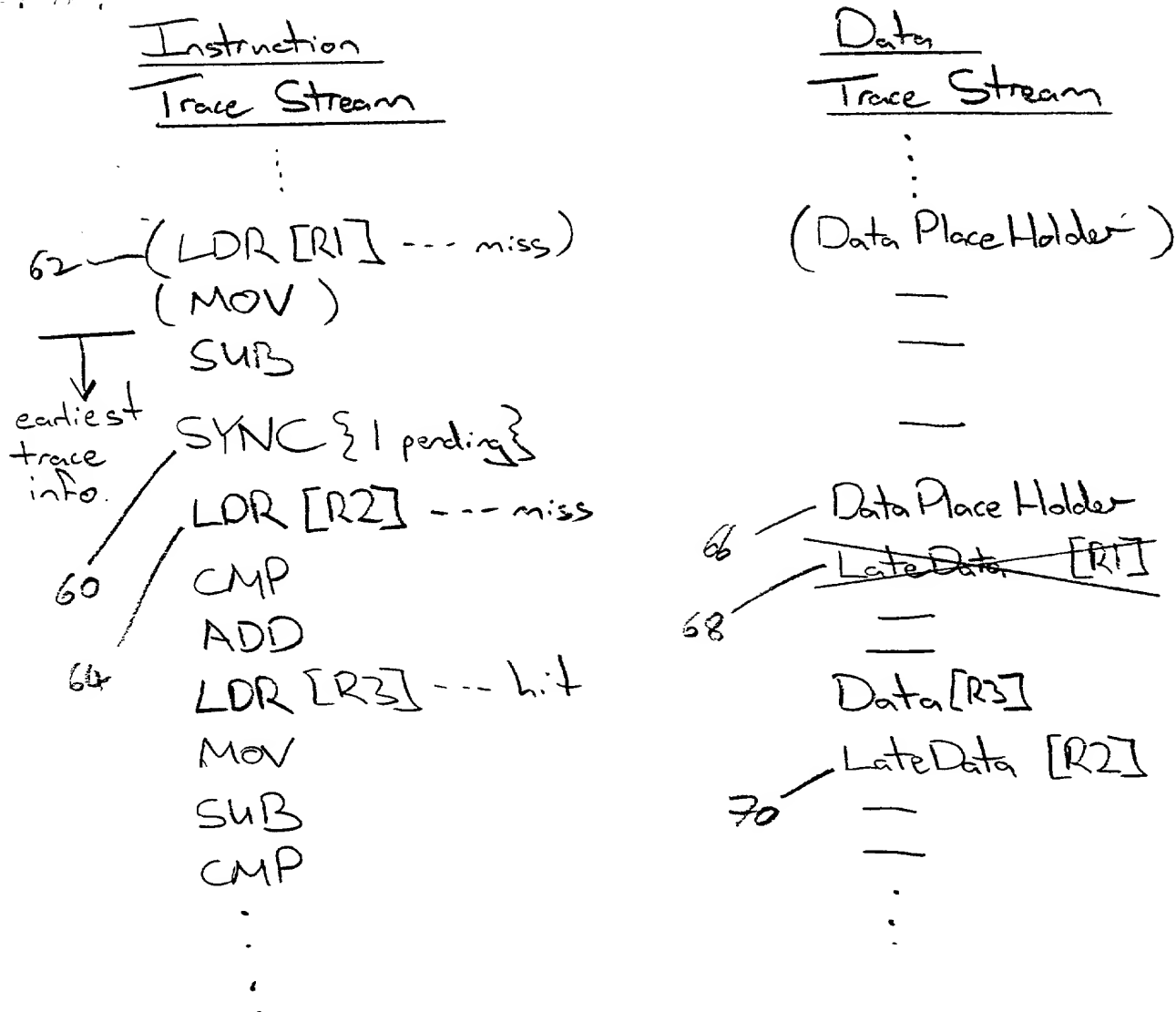


Fig. 5

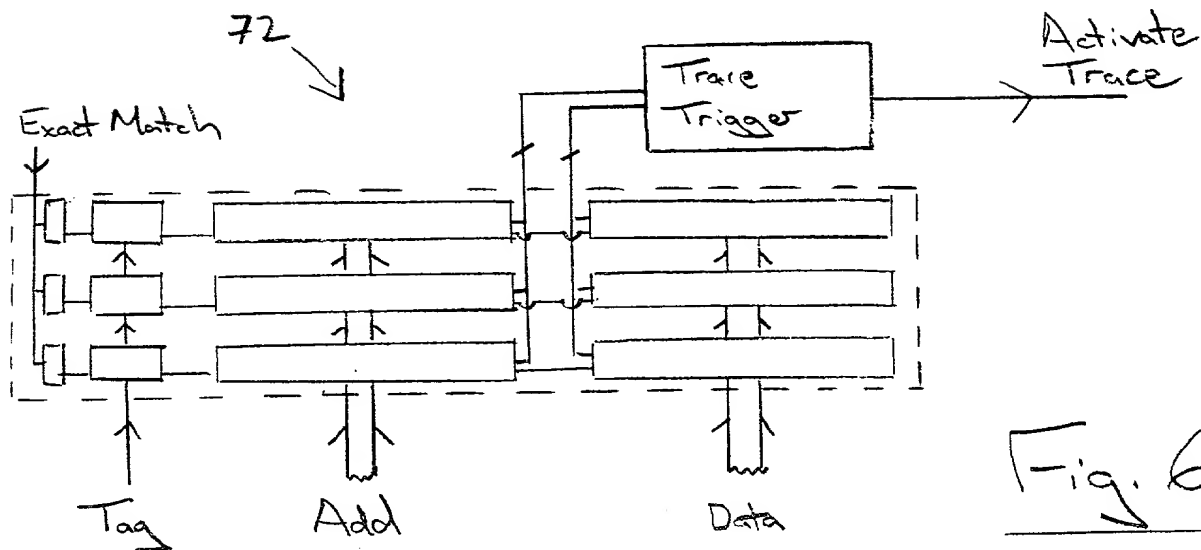


Fig. 6

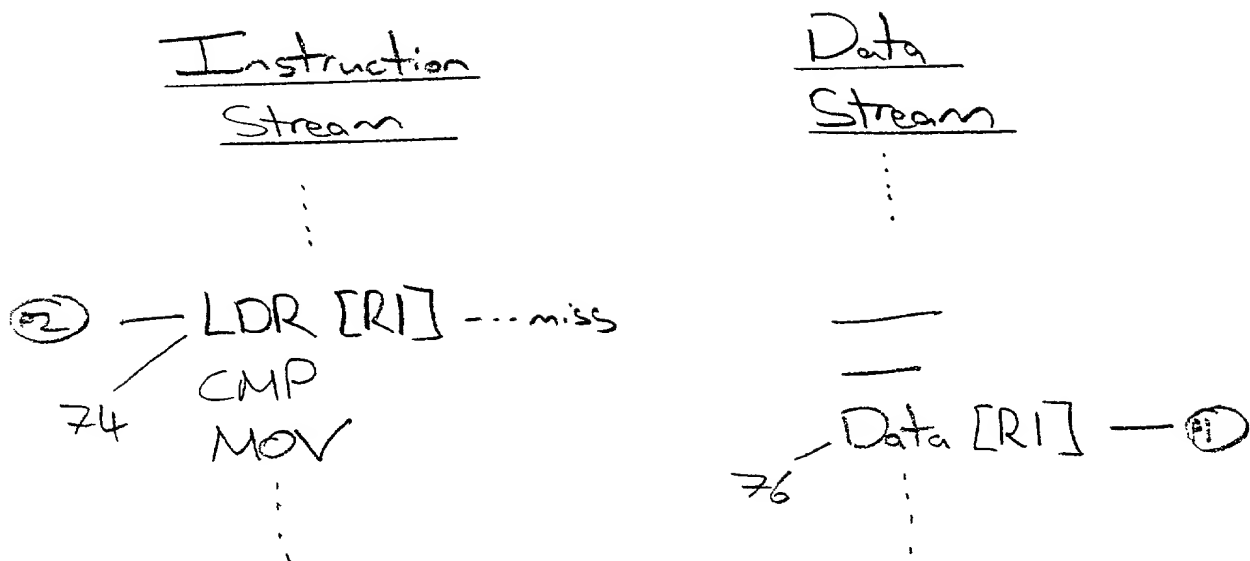


Fig. 7

Exact Match	Add Match	Data Match	Trace Activation Point
✓	✓	✓	①
✓	✓	X	none
X	✓	✓	②
X	✓	X	②

Fig. 8

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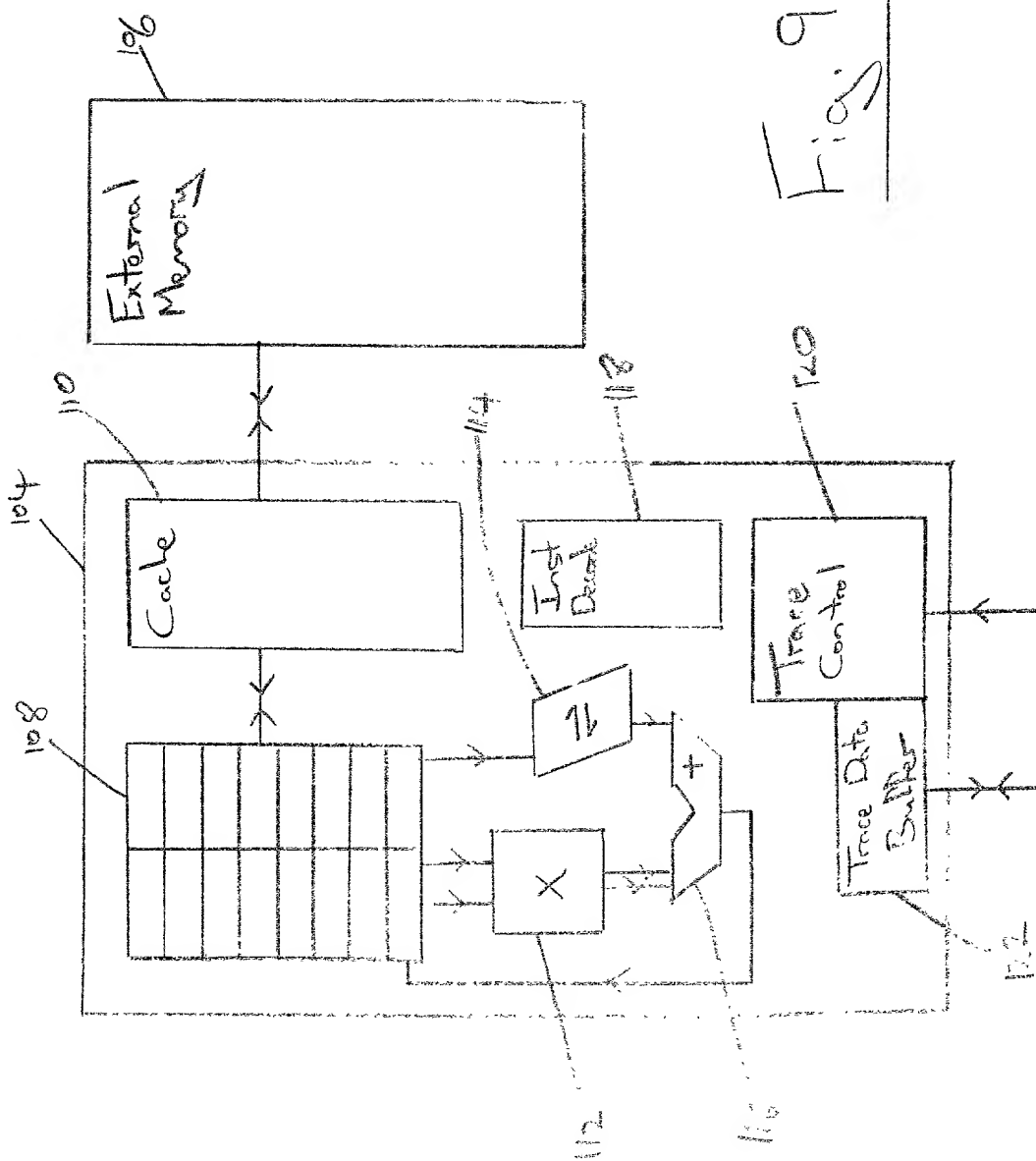


Fig. 9

LSM $R_n[Add], RegList$

16 bits

0000100010001011



R0	
R1	
R3	R11
R7	



\rightarrow
 R0 \leftrightarrow [Add]
 R1 \leftrightarrow [Add+4]
 R3 \leftrightarrow [Add+8]
 R7 \leftrightarrow [Add+12]
 R11 \leftrightarrow [Add+16]

{Add, Add+4, Add+8, Add+12, Add+16}
 {0000, 0004, 0008, 000C, 0010}
 {0000, 0004, 0008, 000C, 0010}

Fig. 10

$$R0 \xleftrightarrow{DW_1} [Add]$$

$$R1 \xleftrightarrow{DW_2} [Add+4]$$

$$R2^{\#} \xleftrightarrow{DW_3^*} [Add+8]$$

$$R7 \xleftrightarrow{DW_4} [Add+12]$$

$$R11 \xleftrightarrow{DW_5} [Add+16]$$

Trace
Traces

Trace
Traces



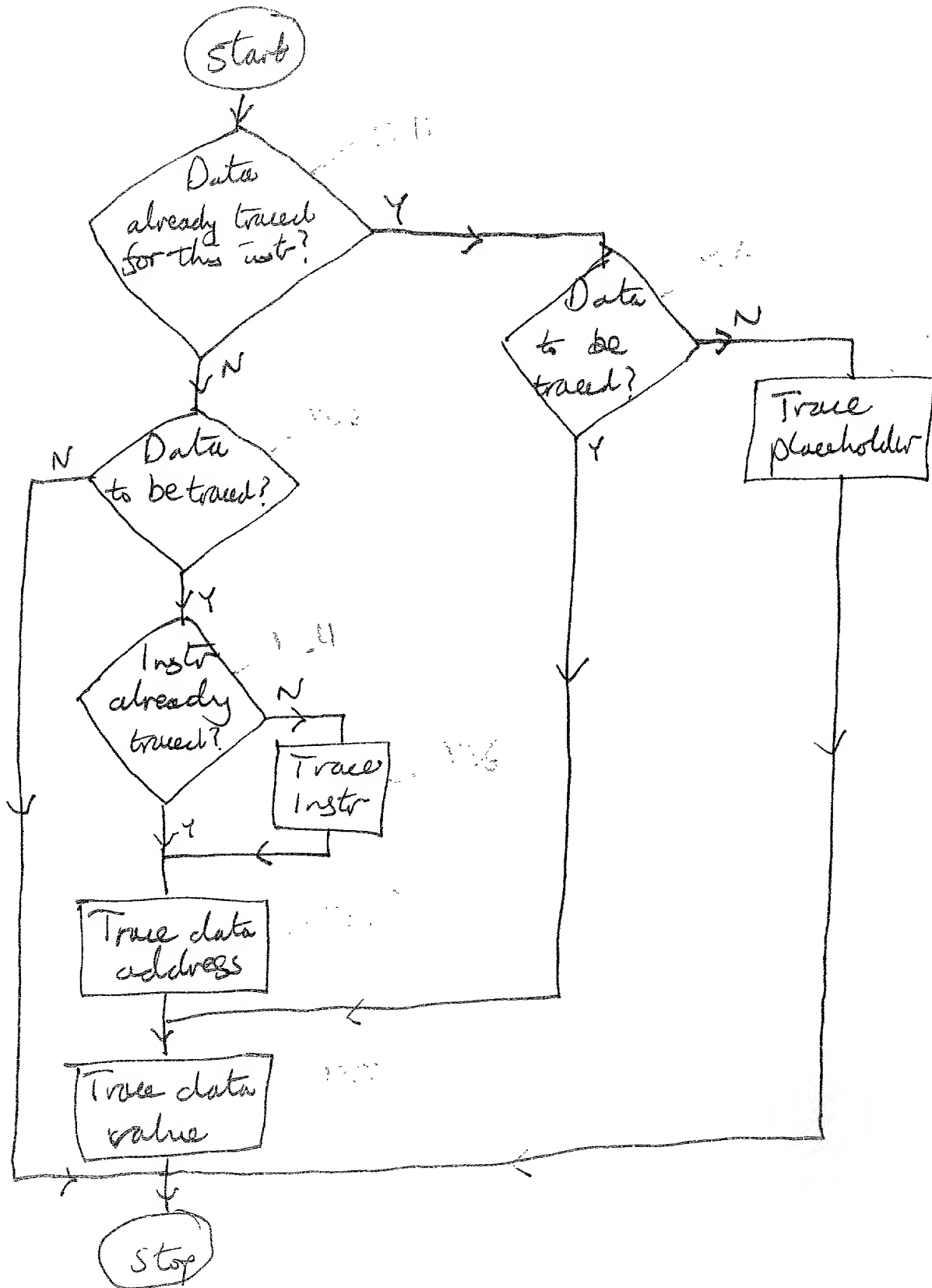
Trace Data Stream

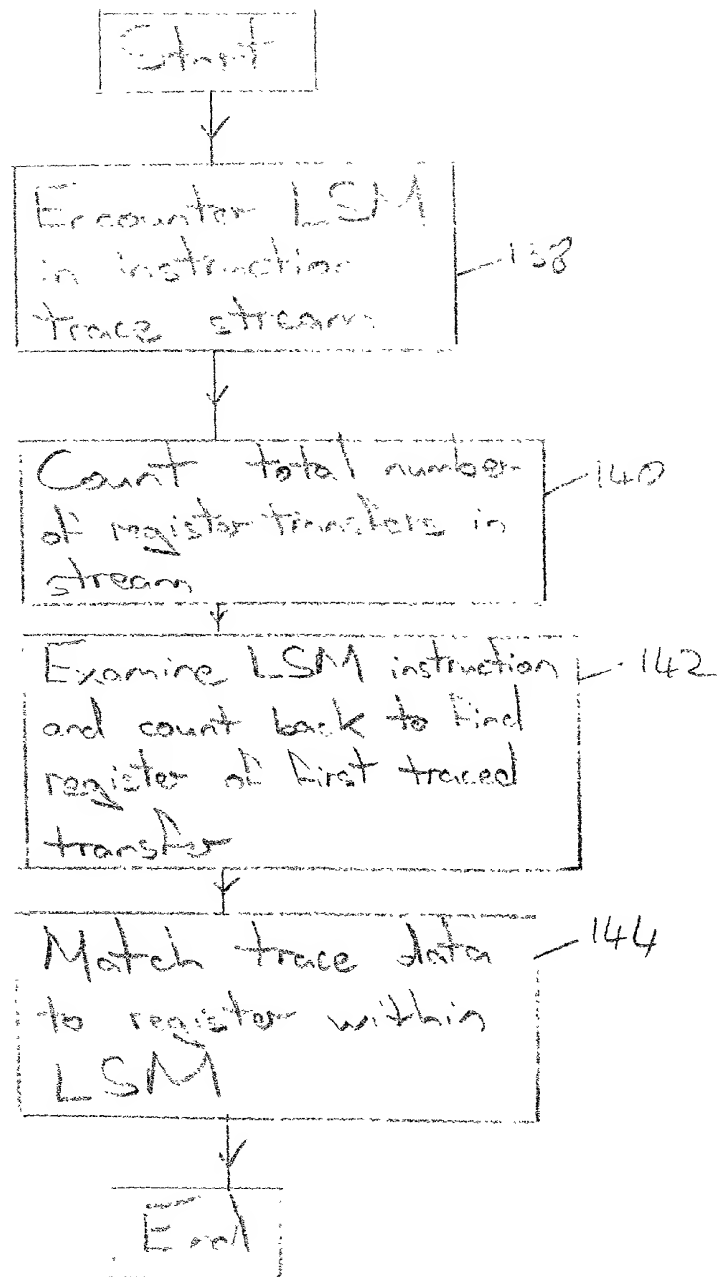
..., {L=0}, {Add+8}, {DW₃}, {Place Holder}, {Place Holder}, ...

Count back to R3

Fig. 1

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[illegible]

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